Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

**2 INPUT VOLTAGE (VIN)**

**4 GND**

**5 TRIM**

**6 OUTPUT VOLTAGE (VOUT)**

**.061”**

**2 6**

**4 5**

**.038”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .038” X .061” DATE: 8/25/21**

**MFG: PMI / ANALOG DEVICES THICKNESS .020” P/N: REF01NBC**

**DG 10.1.2**

#### Rev B, 7/1